AMENDMENTS TO THE SPECIFICATION

Please delete the present fourth full paragraph, appearing on line 15, on page 6 of the specification and replace it with the following new paragraph.

Figure 1 shows a codebook, ~~and~~

Please delete the present fifth full paragraph, appearing on line 16, on page 6 of the specification and replace it with the following new paragraph.

Figure 2 shows a schematic block diagram of an embodiment of the present invention~~,~~

Please add the following new paragraphs after the fifth full paragraph, appearing on line 16 on page 6 of the specification.

Figure 3 shows a schematic diagram of the relationship between the processor and memory, and

Figure 4 shows a schematic diagram of the relationship between the processor and the coder/decoder.

Please delete the present sixth full paragraph, appearing on lines 25-27, on page 7 of the specification and replace it with the following new paragraph.

For each of said two codebook groups CB_0, CB_1, an optimal group code vector is determined in parallel by simultaneously performing a codebook search in the respective codebook group CB_0, CB_1 with an acceleration module 3.

Please delete the present second full paragraph, appearing on lines 10-15, on page 9 of the specification and replace it with the following new paragraph.

To carry out said comparison and to store indices of code vectors already processed, precalculations yielding said cross multiplication expression for each code vector c_t - according to the invention - are carried out in parallel by using specifically designed calculation ~~units~~ unit 4 of a specifically designed digital signal processor (DSP) 1 or coder/decoder 6, with configurable hardware 5. Postcalculations after performing said comparison are also performed in parallel.

Please delete the present fourth full paragraph, appearing on lines 19-20, on page 9 of the specification and replace it with the following new paragraph.

The corresponding computer program controlling the DSP_1 is optimized with respect to parallelism of calculations.

Please delete the present sixth full paragraph, appearing on lines 24-28, on page 10

of the specification and replace it with the following new paragraph.

The signal values of said speech signal s and of said elements of said auto-correlation matrices are represented by 16 bit data words, and since a 64 bit memory read instruction, which is stored in memory 2, is provided by the DSP 1, four signal values located in a memory of said DSP 1 are accessed simultaneously which ensures that even in case of simultaneous evaluation of a plurality of signal values input data is always available.

Please delete the present first full paragraph, appearing on lines 2-4, on page 11 of the specification and replace it with the following new paragraph.

The DSP 1 also has acceleration means implemented on a hardware basis which are specifically designed to evaluate complex expressions that are to be computed repeatedly within few machine cycles.